IN THE CLAIMS

The claims have not been amended herein, but are provided in full for the Examiner's convenience:

1.(Previously Presented) A system comprising:

a processor; and

a memory device coupled to the processor, the memory device comprising:

an array of memory cells comprising a plurality of transistors, at least one of the transistors comprising a source region, a drain region, and a channel region between the source and drain regions in a semiconductor surface layer formed on an underlying insulating portion, and an electrically interconnected gate formed of a silicon carbide compound $Si_{1-x}C_x$, wherein x is less than 0.5, the gate being connected to receive an input signal;

addressing circuitry to address memory cells in the array; and

control circuitry to control read, write, and erase operations of the memory device.

2.(Previously Presented) The system of claim 1 wherein the silicon carbide compound $Si_{1-x}C_x$ comprises polycrystalline silicon carbide or microcrystalline silicon carbide, or both polycrystalline and microcrystalline silicon carbide.

3.(Previously Presented) The system of claim 1 wherein:

the semiconductor surface layer comprises p-type silicon;

the gate is separated from the channel region by gate oxide or tunnel oxide;

the source region comprises n-type silicon; and

the drain region comprises n-type silicon.

4.(Previously Presented) The system of claim 1 wherein:

the semiconductor surface layer comprises n-type silicon;

the gate is separated from the channel region by gate oxide or tunnel oxide;

the source region comprises p-type silicon; and

the drain region comprises p-type silicon.

5.(Previously Presented) The system of claim 1 wherein the silicon carbide compound $Si_{1-x}C_x$ is p+ doped with boron or n+ doped with phosphorus.

6. - 7. (Canceled)

8.(Previously Presented) The system of claim 1 wherein:

the addressing circuitry further comprises:

a row decoder; and

a column decoder;

the memory device further comprises a voltage control switch; and

the system further comprises control lines, address lines, and data lines coupled between the processor and the memory device.

9.(Previously Presented) The system of claim 1 wherein the gate is separated from the channel region by an insulating layer that is approximately between 50 angstroms and 100 angstroms thick.

10.(Previously Presented) The system of claim 9 wherein the insulating layer is approximately 100 angstroms thick.

11. (Original) An integrated circuit device comprising:

a substrate;

a p-channel transistor formed in a first portion of the substrate, the p-channel transistor including a source region, a drain region, a channel region between the source and drain regions, and an electrically interconnected silicon carbide gate over the channel region and separated therefrom by an insulating layer, the gate of the p-channel transistor comprising a silicon carbide compound $Si_{1-x}C_x$, wherein x is less than 0.5, and being connected to receive a first input signal; and

an n-channel transistor formed in a second portion of the substrate, the n-channel transistor including a source region, a drain region, a channel region between the source and drain regions, and an electrically interconnected silicon carbide gate over the channel region and separated therefrom by an insulating layer, the gate of the n-channel transistor comprising a silicon carbide compound $Si_{1-x}C_x$, wherein x is less than 0.5, and being connected to receive a second input signal.

12. (Original) The integrated circuit device of claim 11, wherein the p-channel and n-channel silicon carbide gates comprise polycrystalline silicon carbide.

13. (Original) The integrated circuit device of claim 11, wherein the p-channel and n-channel silicon carbide gates comprise microcrystalline silicon carbide.

14. (Original) The integrated circuit device of claim 11, wherein the insulating layers, which separate the silicon carbide gates in each of the n-channel and p-channel transistors from their respective channel regions, are comprised of silicon dioxide.

15. (Original) A semiconductor memory device comprising:

a memory array including a plurality of transistors, at least one of the transistors in a semiconductor surface layer formed on an underlying insulating portion and including an electrically interconnected gate formed of a silicon carbide compound $Si_{1-x}C_x$, wherein x is less than 0.5, the gate being connected to receive an input signal;

addressing circuitry to address the memory array; and

control circuitry to control read, write, and erase operations of the memory device.

16. - 21. (Canceled)

22. (Original) The integrated circuit device of claim 11 wherein the substrate comprises a semiconductor surface layer formed on an underlying insulating portion.

23. (Canceled)

24. (Original) The semiconductor memory device of claim 15 wherein a plurality of the transistors in the memory array comprise:

a source region, a drain region, and a channel region between the source and drain regions in a semiconductor surface layer formed on an underlying insulating portion; and

an electrically interconnected gate formed of a silicon carbide compound $Si_{1-x}C_x$, wherein x is less than 0.5, the gate being connected to receive an input signal.

25. (Original) The semiconductor memory device of claim 15 wherein pairs of the transistors in the memory array comprise:

a substrate;

a p-channel transistor formed in a first portion of the substrate, the p-channel transistor including a source region, a drain region, a channel region between the source and drain regions, and an electrically interconnected silicon carbide gate over the channel region and separated therefrom by an insulating layer, the gate of the p-channel transistor comprising a silicon carbide compound $Si_{1-x}C_x$, wherein x is less than 0.5, and being connected to receive a first input signal; and

an n-channel transistor formed in a second portion of the substrate, the n-channel transistor including a source region, a drain region, a channel region between the source and drain regions, and an electrically interconnected silicon carbide gate over the channel region and separated therefrom by an insulating layer, the gate of the n-channel transistor comprising a silicon carbide compound $Si_{1-x}C_x$, wherein x is less than 0.5, and being connected to receive a second input signal.

26. (Original) The semiconductor memory device of claim 25 wherein the substrate comprises a semiconductor surface layer formed on an underlying insulating portion.

27. (Original) The semiconductor memory device of claim 15 wherein the silicon carbide compound $Si_{1-x}C_x$ comprises polycrystalline silicon carbide.

28. (Original) The semiconductor memory device of claim 15 wherein the silicon carbide compound $Si_{1-x}C_x$ comprises microcrystalline silicon carbide.

29. (Original) The semiconductor memory device of claim 15 wherein the gate is separated from the semiconductor surface layer by an insulating layer of silicon dioxide.

30. (Canceled)

31. (Original) A semiconductor memory device comprising:

a memory array including a plurality of transistors wherein pairs of the transistors comprise:

a substrate;

a p-channel transistor formed in a first portion of the substrate, the p-channel transistor including a source region, a drain region, a channel region between the source and drain regions, and an electrically interconnected silicon carbide gate over the channel region and separated therefrom by an insulating layer, the gate of the p-channel transistor comprising a silicon carbide compound $Si_{1-x}C_x$, wherein x is less than 0.5, and being connected to receive a first input signal; and

an n-channel transistor formed in a second portion of the substrate, the n-channel transistor including a source region, a drain region, a channel region between the source and drain regions, and an electrically interconnected silicon carbide gate over the channel region and separated therefrom by an insulating layer, the gate of the n-channel transistor comprising a silicon carbide compound $Si_{1-x}C_x$, wherein x is less than 0.5, and being connected to receive a second input signal;

addressing circuitry to address the memory array; and

control circuitry to control read, write, and erase operations of the memory device.

32. (Original) The semiconductor memory device of claim 31 wherein the substrate comprises a semiconductor surface layer formed on an underlying insulating portion.

33. (Original) The semiconductor memory device of claim 31 wherein each silicon carbide gate comprises polycrystalline silicon carbide.

34. (Original) The semiconductor memory device of claim 31 wherein each silicon carbide gate comprises microcrystalline silicon carbide.

35. (Original) The semiconductor memory device of claim 31 wherein each insulating layer comprises silicon dioxide.

36. (Canceled)

37.(Previously Presented) A memory device comprising:

an array of memory cells comprising a plurality of transistors, at least one of the transistors comprising:

a substrate having a source region, a drain region, and a channel region between the source region and the drain region formed in the substrate;

an insulating layer on the substrate over the channel region; and

a gate comprising a p+ doped silicon carbide compound $Si_{1-x}C_x$ on the insulating layer, wherein x is less than 0.5, the gate being electrically interconnected to receive an input signal.

38.(Previously Presented) The memory device of claim 37 wherein:

the substrate comprises a silicon surface layer formed on an underlying insulating portion having a source region, a drain region, and a channel region between the source region and the drain region formed in the silicon surface layer;

the insulating layer comprises gate oxide or tunnel oxide;

the silicon carbide compound $Si_{1-x}C_x$ comprises polycrystalline silicon carbide or microcrystalline silicon carbide, or both polycrystalline and microcrystalline silicon carbide;

the silicon carbide compound $Si_{1-x}C_x$ is p+ doped with boron; and

further comprising:

a row decoder coupled to the array;

a column decoder coupled to the array;

a voltage control switch; and

control circuitry coupled to the array to control read, write, and erase operations of the memory device.

39.(Previously Presented) The memory device of claim 37 wherein:

the substrate comprises p-type silicon;

the source region comprises n-type silicon; and

the drain region comprises n-type silicon.

40.(Previously Presented) The memory device of claim 37 wherein:

the substrate comprises n-type silicon;

the source region comprises p-type silicon; and

the drain region comprises p-type silicon.

41.(Previously Presented) A memory device comprising:

an array of memory cells comprising a plurality of transistors, at least one of the transistors comprising:

a substrate having a source region, a drain region, and a channel region between the source region and the drain region formed in the substrate;

an insulating layer on the substrate over the channel region; and

a gate comprising an n+ doped silicon carbide compound $Si_{1-x}C_x$ on the insulating layer, wherein x is less than 0.5, the gate being electrically interconnected to receive an input signal.

42.(Previously Presented) The memory device of claim 41 wherein:

the substrate comprises a silicon surface layer formed on an underlying insulating portion having a source region, a drain region, and a channel region between the source region and the drain region formed in the silicon surface layer;

the insulating layer comprises gate oxide or tunnel oxide;

the silicon carbide compound $Si_{1-x}C_x$ comprises polycrystalline silicon carbide or microcrystalline silicon carbide, or both polycrystalline and microcrystalline silicon carbide;

the silicon carbide compound $Si_{1-x}C_x$ is n+ doped with phosphorus; and

further comprising:

a row decoder coupled to the array;

a column decoder coupled to the array;

a voltage control switch; and

control circuitry coupled to the array to control read, write, and erase operations of the memory device.

43.(Previously Presented) The memory device of claim 41 wherein:

the substrate comprises p-type silicon;

the source region comprises n-type silicon; and

the drain region comprises n-type silicon.

44.(Previously Presented) The memory device of claim 41 wherein:

the substrate comprises n-type silicon;

the source region comprises p-type silicon; and

the drain region comprises p-type silicon.

45.(Previously Presented) A memory device comprising:

an array of memory cells comprising a plurality of transistors, at least one of the transistors comprising:

a source region, a drain region, and a channel region between the source region and the drain region formed in a semiconductor substrate;

an insulating layer on the semiconductor substrate over the channel region; and

a gate comprising a silicon carbide compound $Si_{1-x}C_x$ on the insulating layer wherein x is less than 0.5, the gate being electrically interconnected to receive an input signal.

46.(Previously Presented) The memory device of claim 45 wherein:

the semiconductor substrate comprises a p-type silicon surface layer formed on an underlying insulating portion;

the insulating layer comprises gate oxide or tunnel oxide;

the silicon carbide compound $Si_{1-x}C_x$ comprises polycrystalline silicon carbide or microcrystalline silicon carbide, or both polycrystalline and microcrystalline silicon carbide;

the source region comprises n-type silicon; and

the drain region comprises n-type silicon.

47.(Previously Presented) The memory device of claim 45 wherein:

the semiconductor substrate comprises an n-type silicon surface layer formed on an underlying insulating portion;

the silicon carbide compound $Si_{1-x}C_x$ comprises polycrystalline silicon carbide or microcrystalline silicon carbide, or both polycrystalline and microcrystalline silicon carbide;

the insulating layer comprises gate oxide or tunnel oxide;

the source region comprises p-type silicon; and

the drain region comprises p-type silicon.

48.(Previously Presented) The memory device of claim 45 wherein the silicon carbide compound $Si_{1-x}C_x$ is p+ doped with boron or n+ doped with phosphorus.

49. (Canceled)

50.(Previously Presented) A system comprising:

a processor; and

a memory device coupled to the processor, the memory device comprising:

an array of memory cells comprising a plurality of transistors, at least one of the transistors comprising:

a source region, a drain region, and a channel region between the source region and the drain region formed in a semiconductor substrate;

an insulating layer on the semiconductor substrate over the channel region; and

a gate comprising a silicon carbide compound $Si_{1-x}C_x$ on the insulating layer wherein x is less than 0.5, the gate being electrically interconnected to receive an input signal.

51.(Previously Presented) The system of claim 50 wherein:

the semiconductor substrate comprises a p-type silicon surface layer formed on an underlying insulating portion;

the insulating layer comprises gate oxide or tunnel oxide;

the silicon carbide compound $Si_{1-x}C_x$ comprises polycrystalline silicon carbide or microcrystalline silicon carbide, or both polycrystalline and microcrystalline silicon carbide;

the source region comprises n-type silicon; and

the drain region comprises n-type silicon.

52.(Previously Presented) The system of claim 50 wherein:

the semiconductor substrate comprises an n-type silicon surface layer formed on an underlying insulating portion;

the silicon carbide compound $Si_{1-x}C_x$ comprises polycrystalline silicon carbide or microcrystalline silicon carbide, or both polycrystalline and microcrystalline silicon carbide;

the insulating layer comprises gate oxide or tunnel oxide;

the source region comprises p-type silicon; and

the drain region comprises p-type silicon.

53.(Previously Presented) The system of claim 50 wherein the silicon carbide compound $Si_{1-x}C_x$ is p+ doped with boron or n+ doped with phosphorus.

54. (Canceled)

55. (Original) The memory device of claim 45, further comprising:

a row decoder coupled to the array;

a column decoder coupled to the array;

a voltage control switch; and

control circuitry coupled to the array to control read, write, and erase operations of the memory device.

56. (Original) The system of claim 50 wherein:

the memory device further comprises:

a row decoder coupled to the array;

a column decoder coupled to the array;

a voltage control switch; and

control circuitry coupled to the array to control read, write, and erase operations of the memory device; and

the system further comprises control lines, address lines, and data lines coupled between the processor and the memory device.

57. (Original) A system comprising:

a processor; and

a memory device coupled to the processor through control lines, address lines, and data lines, the memory device comprising:

an array of memory cells comprising a plurality of transistors, each of the transistors comprising:

a source region, a drain region, and a channel region between the source region and the drain region formed in a semiconductor substrate;

an insulating layer on the semiconductor substrate over the channel region; and

means for controlling current in the channel region based on an input signal;

a row decoder coupled to the array;

a column decoder coupled to the array;

a voltage control switch; and

control circuitry coupled to the array to control read, write, and erase operations of the memory device.